positioning the semiconductor wafer 1 and at least one exposure mask during the fabrication of the semiconductor wafer 1.

IN THE ABSTRACT:

Delete "Figure 2." so as to limit the Abstract to a single paragraph as follow:

A semiconductor wafer (1) has a multitude of chips (5), of which chips (5) each one of a given number of chips (5) is situated in one of a multitude of adjacent exposure fields (2), and further has process control modules (4) which are each arranged in an exposure field (2), namely each in place of at least one chip (5).

REMARKS

This is responsive to the Office Action dated January 14, 2003 in which the Examiner rejects all the pending claims 1- 4 as being anticipated by van der Have (US Patent No. 5,128,737) under 35 USC §102 (b). In addition, the Examiner objects the drawings for lack of the reference number "3" in the Specification, and the Abstract for being not limited to a single paragraph.

Applicants have amended the second paragraph of page 4 of the Specification to include the reference number "3" indicating the two drop-in areas as shown in Figure 1. Applicants believe such amendment is self-evident and does not introduce any new matter. Applicants have also amended the Abstract by deleting "Figure 2.", thus limiting the Abstract to a single paragraph. These amendments are believed to have overcome the objections from the Examiner to the Specification and the Abstract. Furthermore, applicants respectfully traverse the rejection of the Examiner to the claims 1-4 under 35USC §102(b), as explained in detail below.

A brief explanation of the present invention is believed to be helpful in understanding the